ABSTRACT OF THE DISCLOSURE

Flash memory cells are provided with a high-k material interposed between a floating polysilicon gate and a control gate. A tunnel oxide is interposed between the floating polysilicon gate and a substrate. Methods of forming flash memory cells are also provided comprising forming a first polysilicon layer over a substrate. Forming a trench through the first polysilicon layer and into the substrate, and filling the trench with an oxide layer. Depositing a second polysilicon layer over the oxide, such that the bottom of the second polysilicon layer within the trench is above the bottom of the first polysilicon layer, and the top of the second polysilicon layer within the trench is below the top of the first polysilicon layer. The resulting structure may then be planarized using a CMP process. A high-k dielectric layer may then be deposited over the first polysilicon layer. A third polysilicon layer may then be deposited over the high-k dielectric layer and patterned using photoresist to form a flash memory gate structure. During patterning, exposed second polysilicon layer is etched. An etch stop is detected at the completion of removal of the second polysilicon layer. A thin layer of the first polysilicon layer remains, to be carefully removed using a subsequent selective etch process. The high-k dielectric layer may be patterned to allow for formation of non-memory transistors in conjunction with the process of forming the flash memory cells.